Amendments To The Abstract of the Disclosure
MARKED-UP VERSION

The following marked-up version of the amended Abstract is to aid the Examiner in readily identifying the changes:

A clock divider for a DLL circuit ~~can~~ reduces ~~the~~ power consumption by reducing the number of times of **performing** phase comparison in the DLL circuit when a synchronous memory device is in a power-down mode. The clock divider includes M dividers ~~connected in series,~~ and a power-down controller for receiving an output signal of the (M-1)-th divider and an output signal of the M-th divider and selectively outputting the output signals. ~~The respective~~ **Each** divider~~s~~ divide**s** **the** ~~a frequency of a~~ clock signal **frequency** inputted to the ~~respective~~ divider~~s into~~ **by** 1/2~~,~~ ~~and t~~**T**he output signal **frequency** of the power-down controller **is** ~~has a frequency~~ obtained by dividing the frequency of the clock signal inputted to the first divider into $1/2^{M}$ or $1/2^{(M-1)}$ ~~in accordance with a~~ **depending on the** logic level of a control signal**, which is indicative of the power down mode of the memory device**. ~~The output signal of the third divider is selected in the same manner as the conventional clock divider in the case that the memory device is in a non-power-down mode, but the output signal of the fourth divider is selected in the case that the memory device is in the power-down mode in which the power consumption of the memory device is reduced, thereby reducing the current loss of the DLL circuit.~~